Next Generation Circuits for Semiconductor Industry

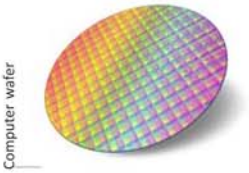
Faster chip performances in electronic devices push CI in nanometer scale


Semiconductor Industry

The scaling required to reach faster chip performances in electronic devices has pushed the dimensions of copper interconnect (CI) lines to the nanometer domain. This constant downscaling of CIs implies a change in their microstructure. A change in the grain boundary type distribution and local texture will strongly influence the resistivity and the mechanical reliability of downscaled CIs. A different texture can imply different mechanical properties and a different local distribution of stresses. It is, therefore, necessary to map the texture evolution with the size of CIs.

Unfortunately, CIs that reach lateral sizes of less than 100 nm, with Cu grains smaller than 50 nm, cannot be characterized by conventional techniques like EBSD and XRD, because they do not have enough spatial resolution.


Circuit with microprocessor


Computer wafer

For reliable texture quantification, it is important to acquire extensive and reliable data sets to have statistically meaningful results and at the same time have a high spatial resolution. ASTAR with a parallel nano-sized beam, coupled with a small precession angle, has the appropriate spatial resolution (1 nm) and the reliable pattern indexing which reduces the 180° ambiguities by sampling reflections from higher order zones (HOLZ). In addition, ASTAR is able to acquire data and index patterns rapidly, which makes it possible to acquire statistically relevant information.

The challenge:	Characterize Copper Interconnect lines (CI) grain boundaries and texture at 1nm scale
Solution:	ASTAR technique coupled with precession electron diffraction

ASTAR orientation maps reveal the evolution of texture as the CI are scaled from CIs from 1.8 µm to 70 nm. In large CIs the Cu grains have a strong <111> fiber texture normal to the trenches (Fig. 1). In the smallest CIs, a <110> texture is observed, normal to the trench while {111} planes are now parallel to the trench sidewalls (Fig. 1). The microstructure also changes from a bamboo-like structure in large CIs into a polygranular structure in small CIs, where a polygranular microstructure is a microstructure in which there are continuous grain boundary paths along the length of the interconnect. In the 70 nm CIs grain size is not uniform and clusters of small grains are formed at the bottom of the trenches. Such clusters of small grains adversely affect the reliability of CIs. In addition, a decrease in the fraction of coherent twin boundaries was observed with decreasing line widths (Fig. 2). Twin boundaries play an important role in the resistivity performance of CIs. These results are crucial to optimize the process of CI fabrication and to understand how to improve their mechanical and electrical properties.

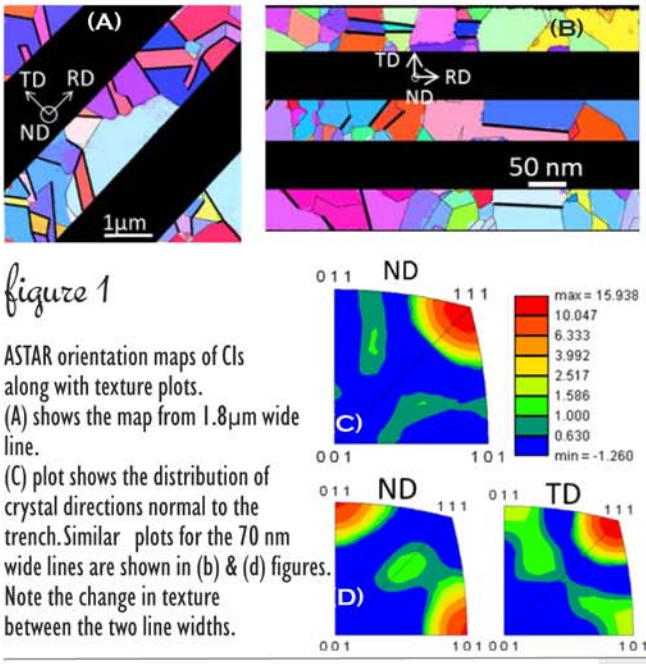


figure 1

ASTAR orientation maps of CIs along with texture plots.
(A) shows the map from 1.8µm wide line.
(C) plot shows the distribution of crystal directions normal to the trench. Similar plots for the 70 nm wide lines are shown in (b) & (d) figures. Note the change in texture between the two line widths.

Experimental Data

TEM type: Jeol 2010 F
Map resolution: 1 nm
Scanned area: 2 x 2 µm

Crystal Structure

Cu: Cubic, $Fm\bar{3}m$
a=3.610 Å

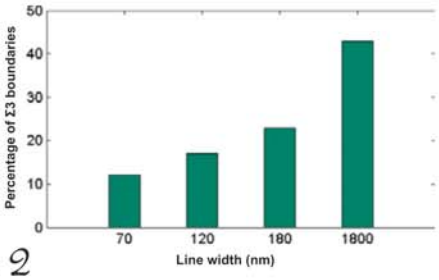


figure 2

Fraction of twin boundaries as a function of line widths. Note the decreasing twin boundary fraction as the line width decreases. Approximately 8000 boundaries extracted from orientation maps was used for this purpose.

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